WHAT IS CLAIMED IS:

1. A buck converter for providing an output voltage to a load, the output voltage being produced from an input voltage in accordance with a desired voltage, the buck converter comprising:

an output capacitor, the output voltage being provided by the output capacitor;

a plurality of output switch arrangements having respective output inductors coupled to the output capacitor, the switch arrangements being controllable to provide respective phase output currents to the output capacitor through the respective output inductors;

a plurality of phase output arrangements respectively coupled to the output switch arrangements, the phase output arrangements being controllable to set the respective phase output currents supplied by the output switch arrangements, each of the phase output arrangements being operable to shutdown the respective output switch arrangement if a signal representing an output current of the buck converter falls below a respective programmable threshold signal; and

a phase control arrangement configured to control the phase output arrangements to set the respective phase output currents supplied by the output switch arrangements so that the output voltage approximates the desired voltage.

2. The buck converter according to claim 1, wherein each of the output switch arrangements includes a high-side switch and a low-side switch coupled to the high-side switch via a respective switch node, the output inductor of each of the output switch arrangements being coupled to the respective switch node.

3. The buck converter according to claim 2, further comprising a phase control bus via which the phase control arrangement controls the phase output arrangements, the phase control bus including a phase timing signal, a PWM control signal, and an average inductor current signal, each of the phase output arrangements includes a start-time arrangement configured to switch on the high-side switch of the respective output switch arrangement in accordance with the phase timing signal, each of the phase output arrangements includes a charge-on duration arrangement configured to switch off the high-side switch of the respective output switch arrangement in accordance with the PWM control signal.

4. The buck converter according to claim 3, wherein the start-time arrangement includes a phase timing comparator electrically coupled to the phase timing signal and a one-shot pulse generator electrically coupled to an output of the phase timing comparator, the one-shot pulse generator configured to produce a clock pulse in accordance with the phase timing signal and a set-point voltage, the clock pulse switching on the high-side switch.

5. The buck converter according to claim 4, wherein the set-point voltage is provided by a voltage divider connected between a reference voltage and a ground voltage.

6. The buck converter according to claim 3, wherein the charge-on duration arrangement includes a ramp generator electrically coupled to the current difference signal and a charge-on duration amplifier electrically coupled to the ramp generator and the PWM control signal, the ramp generator being configured to produce a ramp output signal in accordance with the current difference signal and a default voltage, the charge-on duration amplifier

configured to switch off the high-side switch in accordance with the ramp output signal and the PWM control signal.

7. The buck converter according to claim 6, wherein the ramp generator includes a ramp capacitor electrically coupled to the ramp output signal, a clamp circuit electrically coupled to the ramp output signal and to the default voltage, and a programmable current source electrically coupled between the ramp output signal and a ground voltage, the programmable current source being controllable in accordance with the current difference signal.

8. The buck converter according to claim 7, wherein the phase control bus includes a signal characterizing the desired voltage, each of the phase output arrangements receiving the signal characterizing the desired voltage, the default voltage being set in accordance with the signal characterizing the desired voltage.

9. The buck converter according to claim 7, wherein the ramp generator further includes a phase error detect arrangement configured to produce a phase error signal if the phase output arrangement is incapable of providing a phase output current to match the average inductor current signal.

10. The buck converter according to claim 6, wherein the charge-on duration arrangement further includes a body-brake detect amplifier configured to switch off the high-side switch and the low-side switch in response to at least one of a request for a lower desired voltage and a decrease in a current demand of the load.

11. The buck converter according to claim 10, wherein the request for the lower desired voltage and the decrease in the current demand of the load are determined in accordance with the PWM control signal.

12. The buck converter according to claim 3, wherein each of the phase output arrangements further includes a current sense arrangement electrically connected to a first node and a second node of the respective output inductor and to the average inductor current signal, the current sense arrangement configured to detect the respective phase output current and to generate a current difference signal in accordance with the average inductor current signal and the respective phase output current.

13. The buck converter according to claim 12, wherein the current sense arrangement includes a current detection arrangement connected to the first and second nodes of the respective output inductor and a current comparator electrically connected to an output of the current sense arrangement and to the average inductor current signal, the current sense arrangement generating the current difference signal in accordance with the output of the current sense arrangement and the average inductor current signal.

14. The buck converter according to claim 13, wherein the current detection arrangement includes a current sense amplifier, a resistor R_{CS} electrically coupled between a positive input of the current sense amplifier and the first node, and a capacitor C_{CS} electrically coupled between the positive input and a negative input of the current sense amplifier, the second node being connected to the negative input, a time constant of the

resistor R_{CS} and the capacitor C_{CS} being approximately equal to a time constant of the respective output inductor.

15. The buck converter according to claim 3, wherein the phase control arrangement includes a phase timing arrangement and a PWM arrangement, the phase timing arrangement configured to produce the phase timing signal and the PWM arrangement configured to produce the PWM control signal.

16. The buck converter according to claim 15, wherein the phase timing arrangement includes a programmable oscillator arrangement and a periodic waveform generator electrically coupled to the programmable oscillator arrangement, a frequency of the programmable oscillator arrangement be selectable via a frequency select input, the periodic waveform generator producing the phase timing signal in accordance with the frequency of the programmable oscillator arrangement.

17. The buck converter according to claim 15, wherein the PWM arrangement includes a digital-to-analog converter configured to produce a variable characterizing the desired voltage in accordance with a plurality of digital VID signals, a high-gain error amplifier electrically coupled to the variable characterizing the desired voltage and the output voltage, the high-gain error amplifier producing the PWM control signal in accordance with the variable characterizing the desired voltage and the output voltage.

18. The buck converter according to claim 15, wherein the PWM arrangement further includes droop circuitry configured to modify the PWM control signal, such that the output voltage is reduced proportionally to an increase in a current flow through the load.

19. The buck converter according to claim 15, wherein the PWM arrangement further includes body-brake circuitry configured to modify the PWM control signal, such that the phase output arrangements switch off the high-side and low-side switches of the respective output switch arrangements in response to a request for a lower desired output voltage.

20. The buck converter according to claim 3, wherein each of the phase control arrangement and the phase output arrangements includes a respective over-temperature detect circuit configured to produce a VRHOT signal if a temperature of the respective integrated circuit rises above a respective temperature threshold.

21. The buck converter according to claim 1, wherein the phase output arrangements include a fixed number of phase output arrangements.

22. A phase output arrangement of a buck converter, the phase output arrangement being electrically coupleable to an output switch arrangement having an output inductor, a high-side switch, and a low-side switch, the buck converter providing an output voltage to a load via an output capacitor electrically coupled to the output inductor, the output voltage being produced from an input voltage in accordance with a desired voltage, the phase output arrangement comprising:

an arrangement configured to shutdown the high-side and low-side switches of the output switch arrangement if a signal representing an output current of the buck converter falls below a programable threshold signal.

23. The phase output arrangement according to claim 22, wherein the arrangement configured to shutdown the high-side and low-side switches of the output switch arrangement if the signal representing an output current of the buck converter falls below the programmable threshold signal includes:

a converter output current detect arrangement operable to generate the signal representing the output current of the buck converter; and

a phase shutdown comparator electrically coupled to the signal representing the output current of the buck converter and to the programmable threshold signal, the phase shutdown comparator generating a shutdown signal for shutting down the high-side and low-side switches of the output switch arrangement if the signal representing the output current of the buck converter falls below the programmable threshold signal.

24. The phase output arrangement according to claim 22, wherein the programmable threshold signal is provided by an external circuit.

25. The phase output arrangement according to claim 24, wherein the external circuit includes a voltage divider.

26. The phase output arrangement according to claim 25, wherein the voltage divider includes at least two resistors connected to one another in series between a reference voltage and a ground voltage.

27. The phase output arrangement according to claim 24, wherein the external circuit includes an digital-to-analog converter operable to output the programmable threshold signal.